

# MEMORY

## CMOS

# 1 M × 16 BIT

# FAST PAGE MODE DYNAMIC RAM

## MB81V18160B-50/-60/-50L/-60L

### CMOS 1,048,576 × 16 Bit Fast Page Mode Dynamic RAM

#### ■ DESCRIPTION

The Fujitsu MB81V18160B is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 16-bit increments. The MB81V18160B features a “fast page” mode of operation whereby high-speed random access of up to 1,024 × 16 bits of data within the same row can be selected. The MB81V18160B DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81V18160B is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81V18160B is fabricated using silicon gate CMOS and Fujitsu’s advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81V18160B are not critical and all inputs are LVTTTL compatible.

#### ■ PRODUCT LINE & FEATURES

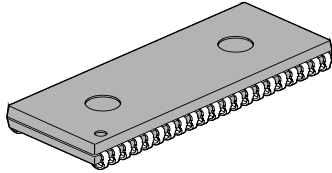
Parameter		MB81V18160B				
		-50	-50L	-60	-60L	
RAS Access Time		60 ns max.		60 ns max.		
Random Cycle Time		90 ns min.		110 ns min.		
Address Access Time		25 ns max.		30 ns max.		
CAS Access Time		13 ns max.		15 ns max.		
Fast Page Mode Cycle Time		35 ns min.		40 ns min.		
Low Power Dissipation	Operating Current	648 mW max.		540 mW max.		
	Standby Current	LVTTTL Level	3.6 mW max.	3.6 mW max.	3.6 mW max.	3.6 mW max.
		CMOS Level	1.8 mW max.	0.54 mW max.	1.8 mW max.	0.54 mW max.

- 1,048,576 words × 16 bit organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are LVTTTL compatible
- 1,024 refresh cycles every 16.4 ms
- Self refresh function (Low power version)
- Standard and low power versions
- Early write or OE controlled write capability
- RAS-only, CAS-before-RAS, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

# MB81V18160B-50/-60/-50L/-60L

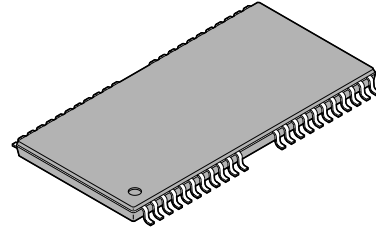
## ■ PACKAGE

42-pin plastic SOJ



(LCC-42P-M01)

50-pin plastic TSOP (II)



(FPT-50P-M06)  
(Normal Bend)

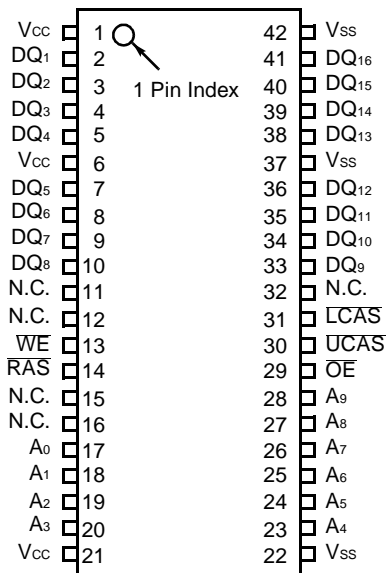
### Package and Ordering Information

- 42-pin plastic (400 mil) SOJ, order as MB81V18160B-xxPJ
- 50-pin plastic (400 mil) TSOP-II with normal bend leads, order as MB81V18160B-xxPFTN and MB81V18160B-xxLPFTN (Low Power)

# MB81V18160B-50/-60/-50L/-60L

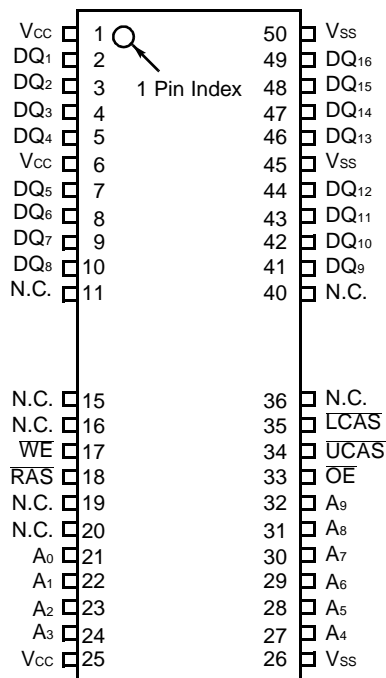
## ■ PIN ASSIGNMENTS AND DESCRIPTIONS

42-Pin SOJ  
(TOP VIEW)  
<LCC-42P-M01>



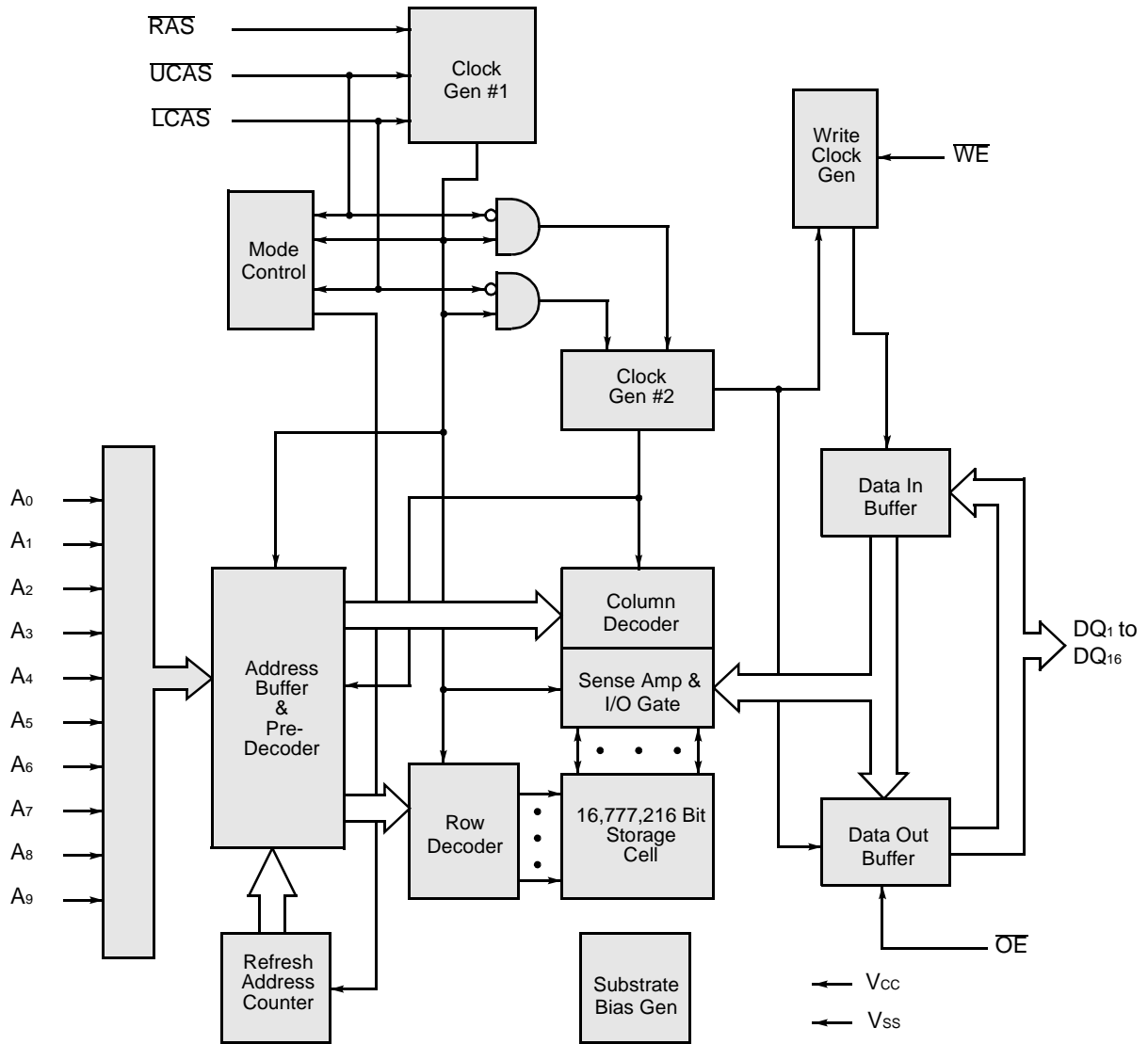
Designator	Function
A <sub>0</sub> to A <sub>9</sub>	Address inputs row: A <sub>0</sub> to A <sub>9</sub> column: A <sub>0</sub> to A <sub>9</sub> refresh: A <sub>0</sub> to A <sub>9</sub>
RAS	Row address strobe
LCAS	Lower column address strobe
UCAS	Upper column address strobe
WE	Write enable
OE	Output enable
DQ <sub>1</sub> to DQ <sub>16</sub>	Data Input/Output
V <sub>CC</sub>	+3.3 volt power supply
V <sub>SS</sub>	Circuit ground
N.C.	No connection

50-Pin TSOP  
(TOP VIEW)  
<Normal Bend: FPT-50P-M06>



# MB81V18160B-50/-60/-50L/-60L

Fig. 1 - MB81V18160B DYNAMIC RAM - BLOCK DIAGRAM



# MB81V18160B-50/-60/-50L/-60L

## FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address Input		Input/Output Data				Refresh	Note
	RAS	LCAS	UCAS	WE	OE	Row	Column	DQ <sub>1</sub> to DQ <sub>8</sub>		DQ <sub>9</sub> to DQ <sub>16</sub>			
								Input	Output	Input	Output		
Standby	H	H	H	X	X	—	—	—	High-Z	—	High-Z	—	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes*	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid — Valid	High-Z	— Valid Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify- Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid — Valid	Valid High-Z Valid	— Valid Valid	High-Z Valid Valid	Yes*	$t_{CWD} \geq t_{CWD}$ (min)
RAS-only Refresh Cycle	L	H	H	X	X	Valid	X	—	High-Z	—	High-Z	Yes	
CAS-before- RAS Refresh Cycle	L	L	L	X	X	X	X	—	High-Z	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H→L	L H L	H L L	H→L	L	X	X	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes	Previous data is kept

X: "H" or "L"

\* : It is impossible in Fast Page Mode.

## FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any sixteen of 16,777,216 cell addresses in the memory matrix. Since only twelve address bits ( $A_0$  to  $A_9$ ) are available, the column and row inputs are separately strobed by  $\overline{LCAS}$  or  $\overline{UCAS}$  and  $\overline{RAS}$  as shown in Figure 1. First, ten row address bits are input on pins  $A_0$ -through- $A_9$  and latched with the row address strobe ( $\overline{RAS}$ ) then, ten column address bits are input and latched with the column address strobe ( $\overline{LCAS}$  or  $\overline{UCAS}$ ). Both row and column addresses must be stable on or before the falling edges of  $\overline{RAS}$  and  $\overline{LCAS}$  or  $\overline{UCAS}$ , respectively. The address latches are of the flow-through type; thus, address information appearing after  $t_{RAH}$  (min) +  $t_t$  is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of  $\overline{WE}$ . When  $\overline{WE}$  is active Low, a write cycle is initiated; when  $\overline{WE}$  is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUTS

Input data is written into memory in either of three basic ways—an early write cycle, an  $\overline{OE}$  (delayed) write cycle, and a read-modify-write cycle. The falling edge of  $\overline{WE}$  or  $\overline{LCAS}/\overline{UCAS}$ , whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data of  $DQ_1$  to  $DQ_8$  is strobed by  $\overline{LCAS}$  and  $DQ_9$  to  $DQ_{16}$  is strobed by  $\overline{UCAS}$  and the setup/hold times are referenced to each  $\overline{LCAS}$  and  $\overline{UCAS}$  because  $\overline{WE}$  goes Low before  $\overline{LCAS}/\overline{UCAS}$ . In a delayed write or a read-modify-write cycle,  $\overline{WE}$  goes Low after  $\overline{LCAS}/\overline{UCAS}$ ; thus, input data is strobed by  $\overline{WE}$  and all setup/hold times are referenced to the write-enable signal.

# MB81V18160B-50/-60/-50L/-60L

## DATA OUTPUTS

The three-state buffers are LVTTTL compatible with a fanout of one TTL load. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- $t_{RAC}$  : from the falling edge of  $\overline{RAS}$  when  $t_{RCD}$  (max) is satisfied.
- $t_{CAC}$  : from the falling edge of  $\overline{LCAS}$  (for DQ<sub>1</sub> to DQ<sub>8</sub>)  $\overline{UCAS}$  (for DQ<sub>9</sub> to DQ<sub>16</sub>) when  $t_{RCD}$  is greater than  $t_{RCD}$  (max).
- $t_{AA}$  : from column address input when  $t_{RAD}$  is greater than  $t_{RAD}$  (max).
- $t_{OEA}$  : from the falling edge of  $\overline{OE}$  when  $\overline{OE}$  is brought Low after  $t_{RAC}$ ,  $t_{CAC}$ , or  $t_{AA}$ , and  $t_{RCD}$  (max) is satisfied.

The data remains valid until either  $\overline{LCAS}/\overline{UCAS}$  or  $\overline{OE}$  returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

## FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions,  $\overline{RAS}$  is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of  $1,024 \times 16$  bits can be accessed and, when multiple MB81V18160Bs are used,  $\overline{CAS}$  is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

# MB81V18160B-50/-60/-50L/-60L

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to +4.6	V
Voltage of $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Power Dissipation	$P_D$	1.0	W
Short Circuit Output Current	$I_{OUT}$	-50 to +50	mA
Operating Temperature	$T_{OPE}$	0 to +70	°C
Storage Temperature	$T_{STG}$	-55 to +125	°C

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Supply Voltage	*1	$V_{CC}$	3.0	3.3	3.6	V	0°C to +70°C
		$V_{SS}$	0	0	0		
Input High Voltage, All Inputs	*1	$V_{IH}$	2.0	—	$V_{CC} + 0.3$ V	V	
Input Low Voltage, All Inputs*	*1	$V_{IL}$	-0.3	—	0.8	V	

\* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ CAPACITANCE

( $T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance, $A_0$ to $A_9$	$C_{IN1}$	5	pF
Input Capacitance, $\overline{RAS}$ , $\overline{LCAS}$ , $\overline{UCAS}$ , $\overline{WE}$ , $\overline{OE}$	$C_{IN2}$	5	pF
Input/Output Capacitance, $DQ_1$ to $DQ_{16}$	$C_{DQ}$	7	pF

# MB81V18160B-50/-60/-50L/-60L

## ■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note 3

Parameter	Notes	Symbol	Conditions	Value				Unit
				Min.	Typ.	Max.		
						Std power	Low power	
Output High Voltage	*1	$V_{OH}$	$I_{OH} = -2.0 \text{ mA}$	2.4	—	—	—	V
Output Low Voltage	*1	$V_{OL}$	$I_{OL} = +2.0 \text{ mA}$	—	—	0.4	0.4	
Input Leakage Current (Any Input)		$I_{I(L)}$	$0 \text{ V} \leq V_{IN} \leq V_{CC}$ ; $3.0 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$ ; $V_{SS} = 0 \text{ V}$ ; All other pins not under test = $0 \text{ V}$	-10	—	10	10	$\mu\text{A}$
Output Leakage Current		$I_{DO(L)}$	$0 \text{ V} \leq V_{OUT} \leq V_{CC}$ ; $3.0 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$ ; Data out disabled	-10	—	10	10	
Operating Current (Average Power Supply Current)	*2	MB81V18160B -50/50L	$\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ , $\overline{\text{UCAS}}$ cycling; $t_{RC} = \text{min}$	—	—	180	180	mA
		MB81V18160B -60/60L				150	150	
Standby Current (Power Supply Current)	*2	LVTTTL Level	$\overline{\text{RAS}} = \overline{\text{CAS}}$ , $\overline{\text{UCAS}} = V_{IH}$	—	—	1.0	1.0	mA
		CMOS Level	$\overline{\text{RAS}} = \overline{\text{CAS}}$ , $\overline{\text{UCAS}} \geq V_{CC} - 0.2 \text{ V}$			500	150	
Refresh Current#1 (Average Power Supply Current)	*2	MB81V18160B -50/50L	$\overline{\text{CAS}}$ , $\overline{\text{UCAS}} = V_{IH}$ , $\overline{\text{RAS}}$ cycling; $t_{RC} = \text{min}$	—	—	180	180	mA
		MB81V18160B -60/60L				150	150	
Fast Page Mode Current	*2	MB81V18160B -50/50L	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ , $\overline{\text{UCAS}}$ cycling; $t_{PC} = \text{min}$	—	—	110	110	mA
		MB81V18160B -60/60L				100	100	
Refresh Current#2 (Average Power Supply Current)	*2	MB81V18160B -50/50L	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ ; $t_{RC} = \text{min}$	—	—	180	180	mA
		MB81V18160B -60/60L				150	150	
Battery Backup Current (Average Power Supply Current)	*2	MB81V18160B -50/60	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ ; $t_{RC} = 16 \mu\text{s}$ $t_{RAS} = \text{min to } 300 \text{ ns}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IL} \leq 0.2 \text{ V}$	—	—	2000	—	$\mu\text{A}$
		MB81V18160B -50L/60L	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ ; $t_{RC} = 128 \mu\text{s}$ $t_{RAS} = \text{min to } 300 \text{ ns}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IL} \leq 0.2 \text{ V}$			—	300	
Refresh Current#3 (Average Power Supply Current)		MB81V18160B -50L/60L	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}} = V_{IL}$ Self refresh;	—	—	—	250	$\mu\text{A}$



# MB81V18160B-50/-60/-50L/-60L

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V18160B-50/50L		MB81V18160B-60/60L		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh	Std power	t <sub>REF</sub>	—	16.4	—	16.4	ms
		Low power		—	128	—	128	
2	Random Read/Write Cycle Time		t <sub>RC</sub>	90	—	110	—	ns
3	Read-Modify-Write Cycle Time		t <sub>RWC</sub>	126	—	150	—	ns
4	Access Time from $\overline{\text{RAS}}$	*6,9	t <sub>RAC</sub>	—	50	—	60	ns
5	Access Time from $\overline{\text{CAS}}$	*7,9	t <sub>CAC</sub>	—	13	—	15	ns
6	Column Address Access Time	*8,9	t <sub>AA</sub>	—	25	—	30	ns
7	Output Hold Time		t <sub>OH</sub>	3	—	3	—	ns
8	Output Buffer Turn On Delay Time		t <sub>ON</sub>	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	*10	t <sub>OFF</sub>	—	13	—	15	ns
10	Transition Time		t <sub>T</sub>	3	50	3	50	ns
11	$\overline{\text{RAS}}$ Precharge Time		t <sub>RP</sub>	30	—	40	—	ns
12	$\overline{\text{RAS}}$ Pulse Width		t <sub>RAS</sub>	50	100000	60	100000	ns
13	$\overline{\text{RAS}}$ Hold Time		t <sub>RSH</sub>	13	—	15	—	ns
14	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t <sub>CRP</sub>	5	—	5	—	ns
15	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	*11,12	t <sub>RCD</sub>	17	37	20	45	ns
16	$\overline{\text{CAS}}$ Pulse Width		t <sub>CAS</sub>	13	—	15	—	ns
17	$\overline{\text{CAS}}$ Hold Time		t <sub>CSH</sub>	50	—	60	—	ns
18	$\overline{\text{CAS}}$ Precharge Time (Normal)	*19	t <sub>CPN</sub>	7	—	10	—	ns
19	Row Address Setup Time		t <sub>ASR</sub>	0	—	0	—	ns
20	Row Address Hold Time		t <sub>RAH</sub>	7	—	10	—	ns
21	Column Address Setup Time		t <sub>ASC</sub>	0	—	0	—	ns
22	Column Address Hold Time		t <sub>CAH</sub>	7	—	10	—	ns
23	Column Address Hold Time from $\overline{\text{RAS}}$		t <sub>AR</sub>	24	—	30	—	ns
24	$\overline{\text{RAS}}$ to Column Address Delay Time	*13	t <sub>RAD</sub>	12	25	15	30	ns
25	Column Address to $\overline{\text{RAS}}$ Lead Time		t <sub>RAL</sub>	25	—	30	—	ns
26	Column Address to $\overline{\text{CAS}}$ Lead Time		t <sub>CAL</sub>	25	—	30	—	ns
27	Read Command Setup Time		t <sub>RCS</sub>	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	*14	t <sub>RRH</sub>	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	*14	t <sub>RCH</sub>	0	—	0	—	ns
30	Write Command Setup Time	*15,20	t <sub>WCS</sub>	0	—	0	—	ns
31	Write Command Hold Time		t <sub>WCH</sub>	7	—	10	—	ns
32	Write Command Hold Time from $\overline{\text{RAS}}$		t <sub>WCR</sub>	24	—	30	—	ns
33	$\overline{\text{WE}}$ Pulse Width		t <sub>WP</sub>	7	—	10	—	ns
34	Write Command to $\overline{\text{RAS}}$ Lead Time		t <sub>RWL</sub>	13	—	15	—	ns
35	Write Command to $\overline{\text{CAS}}$ Lead Time		t <sub>CWL</sub>	13	—	15	—	ns

(Continued)

# MB81V18160B-50/-60/-50L/-60L

(Continued)

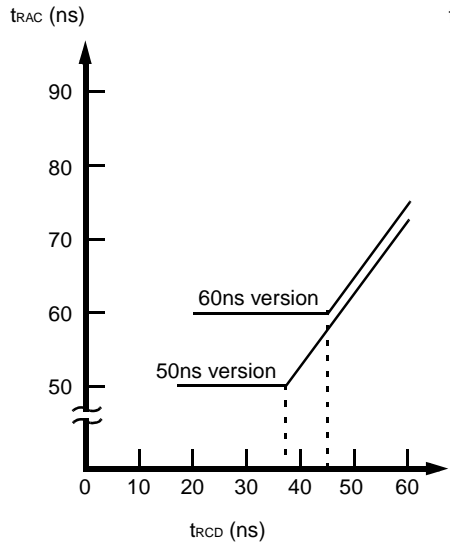
No.	Parameter	Notes	Symbol	MB81V18160B-50/50L		MB81V18160B-60/60L		Unit
				Min.	Max.	Min.	Max.	
36	DIN Setup Time		t <sub>DS</sub>	0	—	0	—	ns
37	DIN Hold Time		t <sub>DH</sub>	7	—	10	—	ns
38	Data Hold Time from $\overline{\text{RAS}}$		t <sub>DHR</sub>	24	—	30	—	ns
39	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	*20	t <sub>RWD</sub>	68	—	80	—	ns
40	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	*20	t <sub>CWD</sub>	31	—	35	—	ns
41	Column Address to $\overline{\text{WE}}$ Delay Time	*20	t <sub>AWD</sub>	43	—	50	—	ns
42	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh Cycles)		t <sub>RPC</sub>	5	—	5	—	ns
43	$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh		t <sub>CSR</sub>	0	—	0	—	ns
44	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh		t <sub>CHR</sub>	10	—	10	—	ns
45	Access time from $\overline{\text{OE}}$	*9	t <sub>OEA</sub>	—	13	—	15	ns
46	Output Buffer Turn Off Delay from $\overline{\text{OE}}$	*10	t <sub>OEZ</sub>	—	13	—	15	ns
47	$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Lead Time for Valid Data		t <sub>OEL</sub>	5	—	5	—	ns
48	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$	*16	t <sub>OEH</sub>	5	—	5	—	ns
49	$\overline{\text{OE}}$ to Data In Delay Time		t <sub>OED</sub>	13	—	15	—	ns
50	$\overline{\text{CAS}}$ to Data In Delay Time		t <sub>CDD</sub>	13	—	15	—	ns
51	DIN to $\overline{\text{CAS}}$ Delay Time	*17	t <sub>DZC</sub>	0	—	0	—	ns
52	DIN to $\overline{\text{OE}}$ Delay Time	*17	t <sub>DZO</sub>	0	—	0	—	ns
53	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width		t <sub>RASP</sub>	—	100000	—	100000	ns
54	Fast Page Mode Read/Write Cycle Time		t <sub>PC</sub>	35	—	40	—	ns
55	Fast Page Mode Read-Modify-Write Cycle Time		t <sub>PRWC</sub>	71	—	80	—	ns
56	Access Time from $\overline{\text{CAS}}$ Precharge	*9,18	t <sub>CPA</sub>	—	30	—	35	ns
57	Fast Page Mode $\overline{\text{CAS}}$ Precharge Time		t <sub>CP</sub>	7	—	10	—	ns
58	Fast Page Mode $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge		t <sub>RHCP</sub>	30	—	35	—	ns
59	Fast Page Mode $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	*20	t <sub>CPWD</sub>	48	—	55	—	ns

# MB81V18160B-50/-60/-50L/-60L

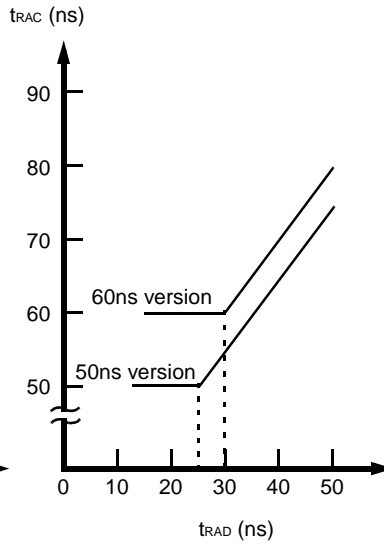
- Notes:**
- \*1. Referenced to  $V_{SS}$ .
  - \*2.  $I_{CC}$  depends on the output load conditions and cycle rates; the specified values are obtained with the output open.  
 $I_{CC}$  depends on the number of address change as  $\overline{RAS} = V_{IL}$ ,  $\overline{UCAS} = V_{IH}$ ,  $\overline{LCAS} = V_{IH}$  and  $V_{IL} > -0.3$  V.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC5}$  are specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{UCAS} = V_{IH}$ ,  $\overline{LCAS} = V_{IH}$ .  
 $I_{CC2}$  is specified during  $\overline{RAS} = V_{IH}$  and  $V_{IL} > -0.3$  V.  
 $I_{CC6}$  is measured on condition that all address signals are fixed steady state.
  - \*3. An initial pause ( $\overline{RAS} = \overline{CAS} = V_{IH}$ ) of 200  $\mu$ s is required after power-up followed by any eight  $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
  - \*4. AC characteristics assume  $t_T = 5$  ns.
  - \*5. Input voltage levels are 0 V and 3.0 V, and input reference levels are  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  for measuring timing of input signals. Also, the transition time ( $t_T$ ) is measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$ . The output reference levels are  $V_{OH} = 2.0$  V and  $V_{OL} = 0.8$  V.
  - \*6. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$ ,  $t_{RAD} \leq t_{RAD}(\text{max})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds the value shown. Refer to Fig.2 and 3.
  - \*7. If  $t_{RCD} \geq t_{RCD}(\text{max})$ ,  $t_{RAD} \geq t_{RAD}(\text{max})$ , and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{CAC}$ .
  - \*8. If  $t_{RAD} \geq t_{RAD}(\text{max})$  and  $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{AA}$ .
  - \*9. Measured with a load equivalent to one TTL load and 100 pF.
  - \*10.  $t_{OFF}$  and  $t_{OEZ}$  are specified that output buffer change to high-impedance state.
  - \*11. Operation within the  $t_{RCD}(\text{max})$  limit ensures that  $t_{RAC}(\text{max})$  can be met.  $t_{RCD}(\text{max})$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  - \*12.  $t_{RCD}(\text{min}) = t_{RAH}(\text{min}) + 2t_T + t_{ASC}(\text{min})$ .
  - \*13. Operation within the  $t_{RAD}(\text{max})$  limit ensures that  $t_{RAC}(\text{max})$  can be met.  $t_{RAD}(\text{max})$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  - \*14. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
  - \*15.  $t_{WCS}$  is specified as a reference point only. If  $t_{WCS} \geq t_{WCS}(\text{min})$  the data output pin will remain High-Z state through entire cycle.
  - \*16. Assumes that  $t_{WCS} < t_{WCS}(\text{min})$ .
  - \*17. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
  - \*18.  $t_{CPA}$  is access time from the selection of a new column address (that is caused by changing both  $\overline{UCAS}$  and  $\overline{LCAS}$  from "L" to "H"). Therefore, if  $t_{CP}$  is long,  $t_{CPA}$  is longer than  $t_{CPA}(\text{max})$ .
  - \*19. Assumes that  $\overline{CAS}$ -before- $\overline{RAS}$  refresh.
  - \*20.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle and DQ pin will maintain high-impedance state throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}(\text{min})$ ,  $t_{RWD} \geq t_{RWD}(\text{min})$ , and  $t_{AWD} \geq t_{AWD}(\text{min})$ ,  $t_{CPWD} \geq t_{CPWD}(\text{min})$ , the cycle is a read-modify-write cycle and data from the selected cell will appear at the DQ pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the DQ pin, and write operation can be executed by satisfying  $t_{RWL}$ ,  $t_{CWL}$ , and  $t_{RAL}$  specifications.

# MB81V18160B-50/-60/-50L/-60L

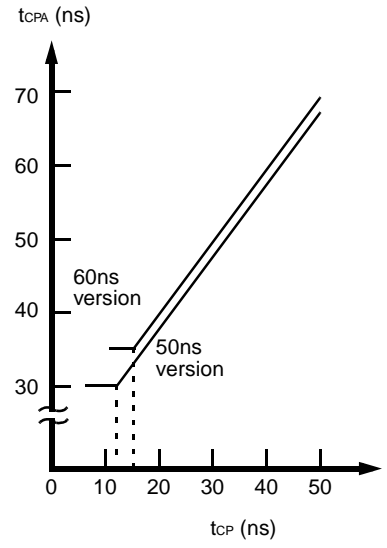
**Fig. 2 -  $t_{RAC}$  vs.  $t_{RCD}$**



**Fig. 3 -  $t_{RAC}$  vs.  $t_{RAD}$**

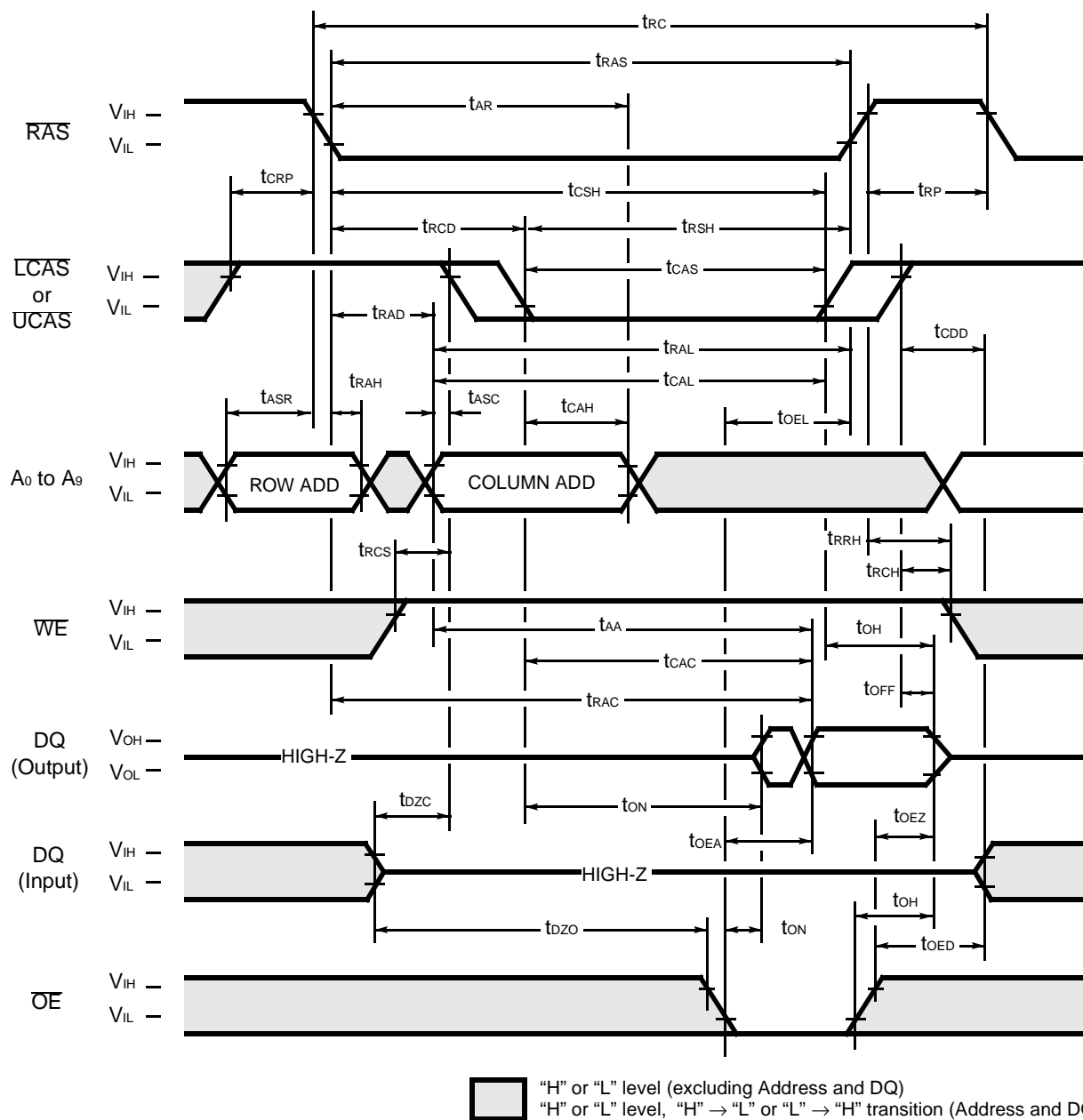


**Fig. 4 -  $t_{CPA}$  vs.  $t_{CP}$**



## MB81V18160B-50/-60/-50L/-60L

Fig. 5 - READ CYCLE

**DESCRIPTION**

To implement a read operation, a valid address is latched by the  $\overline{RAS}$  and  $\overline{LCAS}$  or  $\overline{UCAS}$  address strobes and with  $\overline{WE}$  set to a High level and  $\overline{OE}$  set to a low level, the output is valid once the memory access time has elapsed.  $\overline{LCAS}$  controls the input/output data on DQ<sub>1</sub> to DQ<sub>8</sub> pins,  $\overline{UCAS}$  controls one on DQ<sub>8</sub> to DQ<sub>16</sub> pins. The access time is determined by  $\overline{RAS}$ ( $t_{RAS}$ ),  $\overline{LCAS}/\overline{UCAS}$ ( $t_{CAC}$ ),  $\overline{OE}$ ( $t_{OEA}$ ) or column addresses ( $t_{AA}$ ) under the following conditions:

If  $t_{RCD} > t_{RCD(max)}$ , access time =  $t_{CAC}$ .

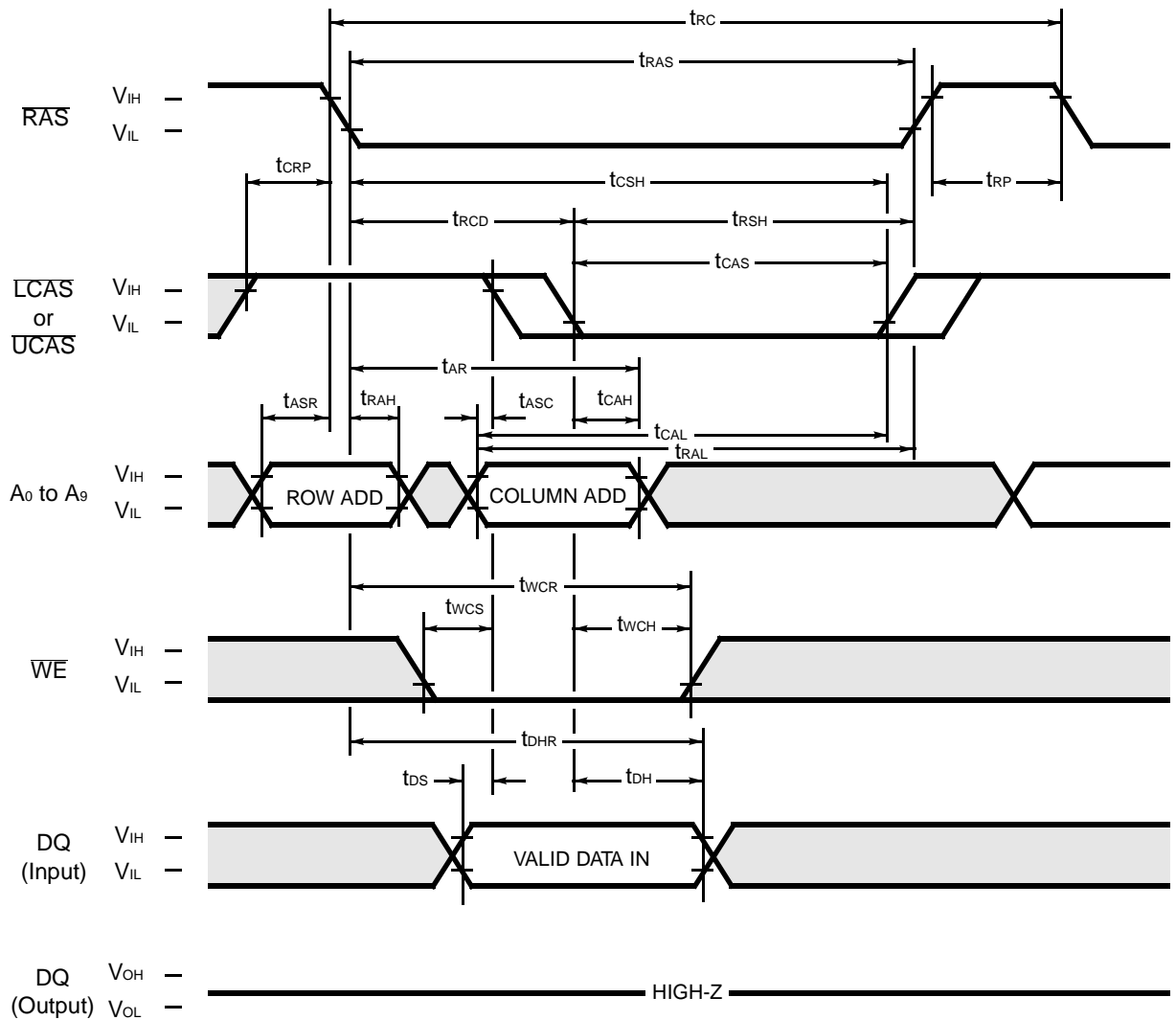
If  $t_{RAD} > t_{RAD(max)}$ , access time =  $t_{AA}$ .

If  $\overline{OE}$  is brought Low after  $t_{RAS}$ ,  $t_{CAC}$ , or  $t_{AA}$ (whichever occurs later), access time =  $t_{OEA}$ .

However, if either  $\overline{LCAS}/\overline{UCAS}$  or  $\overline{OE}$  goes High, the output returns to a high-impedance state after  $t_{OH}$  is satisfied.

# MB81V18160B-50/-60/-50L/-60L

Fig. 6 – EARLY WRITE CYCLE ( $\overline{OE}$  = “H” or “L”)



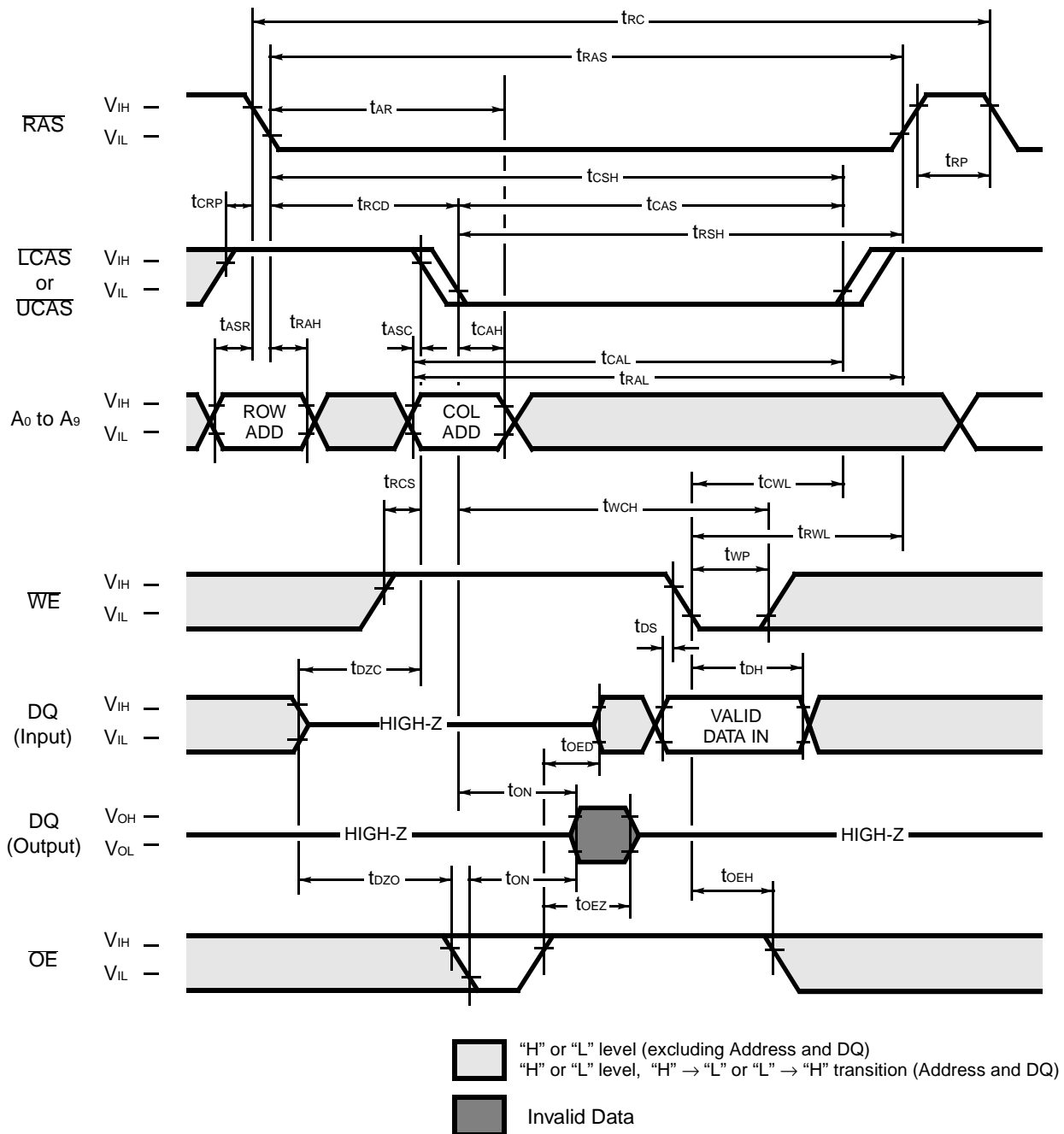
“H” or “L” level (excluding Address and DQ)  
 “H” or “L” level, “H” → “L” or “L” → “H” transition (Address and DQ)

## DESCRIPTION

A write cycle is similar to a read cycle except WE is set to a Low state and  $\overline{OE}$  is an “H” or “L” signal. A write cycle can be implemented in either of three ways – early write, delayed write, or read-modify-write. During all write cycles, timing parameters  $t_{RWL}$ ,  $t_{CWL}$ ,  $t_{RAL}$  and  $t_{CAL}$  must be satisfied. In the early write cycle shown above  $t_{WCS}$  satisfied, data on the DQ pins are latched with the falling edge of LCAS or UCAS and written into memory.

## MB81V18160B-50/-60/-50L/-60L

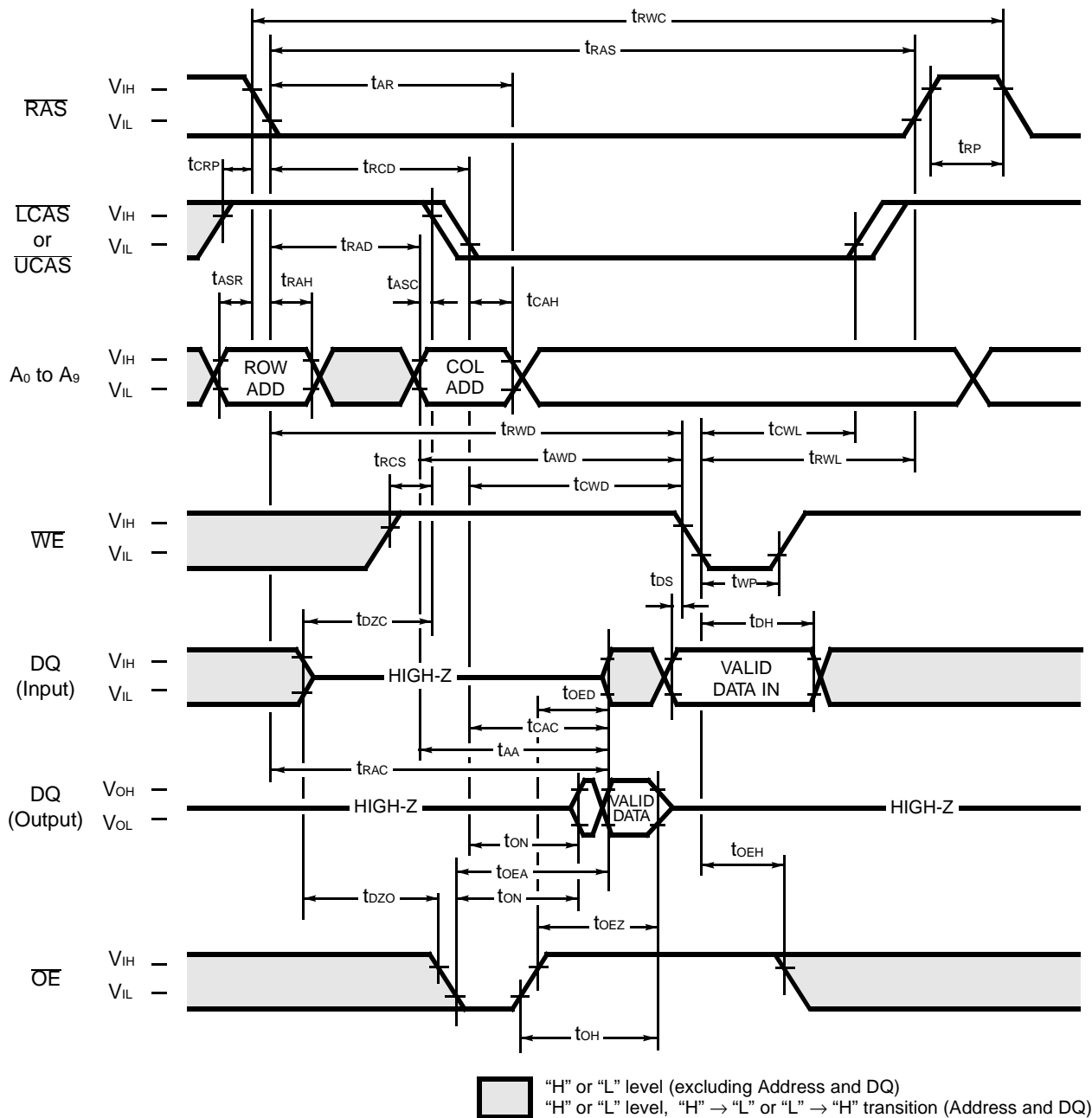
Fig. 7 - DELAYED WRITE CYCLE

**DESCRIPTION**

In the delayed write cycle,  $t_{WCS}$  is not satisfied; thus, the data on the DQ pins is latched with the falling edge of  $\overline{WE}$  and written into memory. The Output Enable ( $\overline{OE}$ ) signal must be changed from Low to High before  $\overline{WE}$  goes Low ( $t_{OED} + t_r + t_{DS}$ ).

## MB81V18160B-50/-60/-50L/-60L

Fig. 8 – READ-MODIFY-WRITE CYCLE

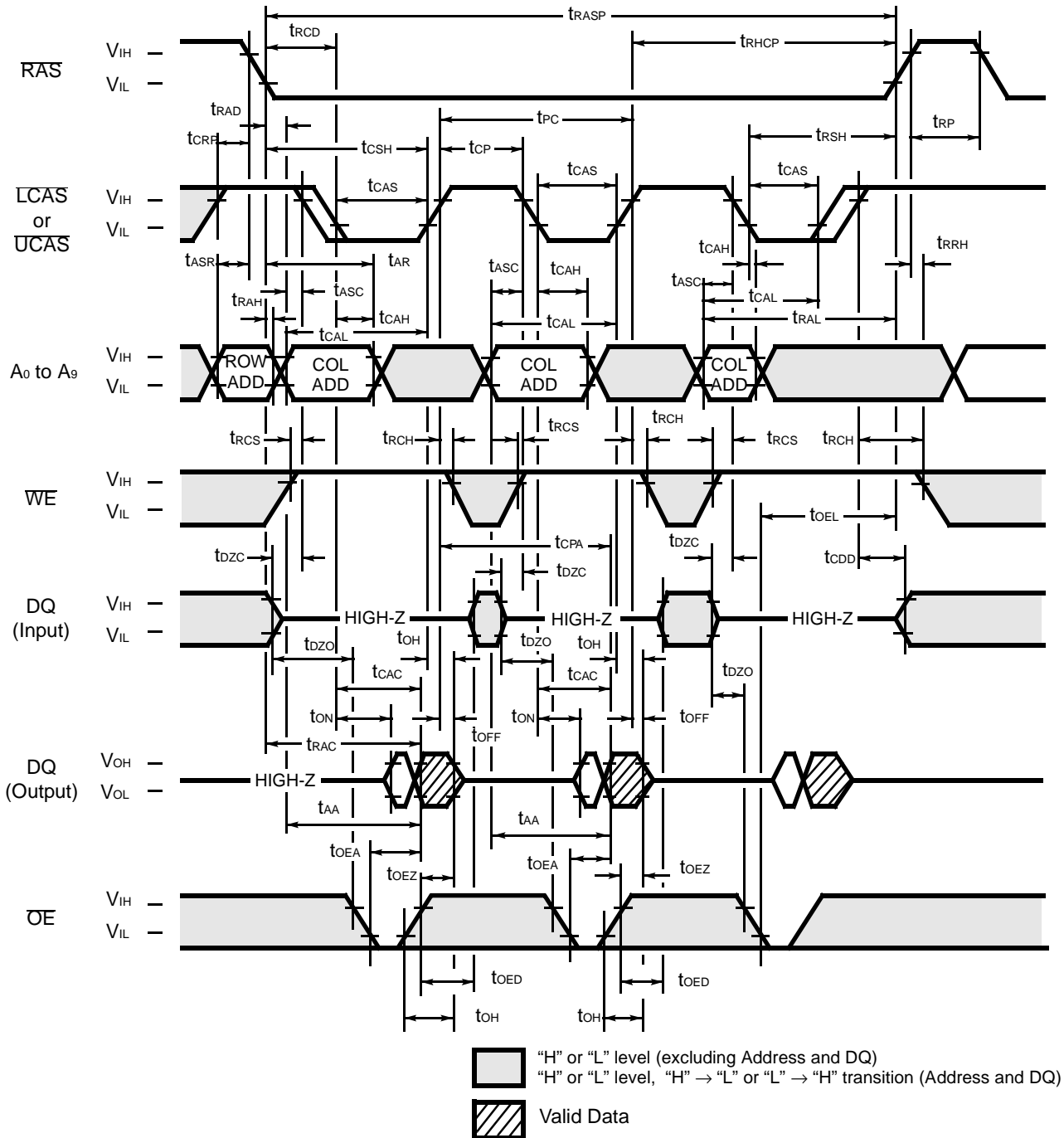
**DESCRIPTION**

The read-modify-write cycle is executed by changing  $\overline{WE}$  from High to Low after the data appears on the DQ pins. In the read-modify-write cycle,  $\overline{OE}$  must be changed from Low to High after the memory access time.



# MB81V18160B-50/-60/-50L/-60L

**Fig. 9 - FAST PAGE MODE READ CYCLE**



**DESCRIPTION**

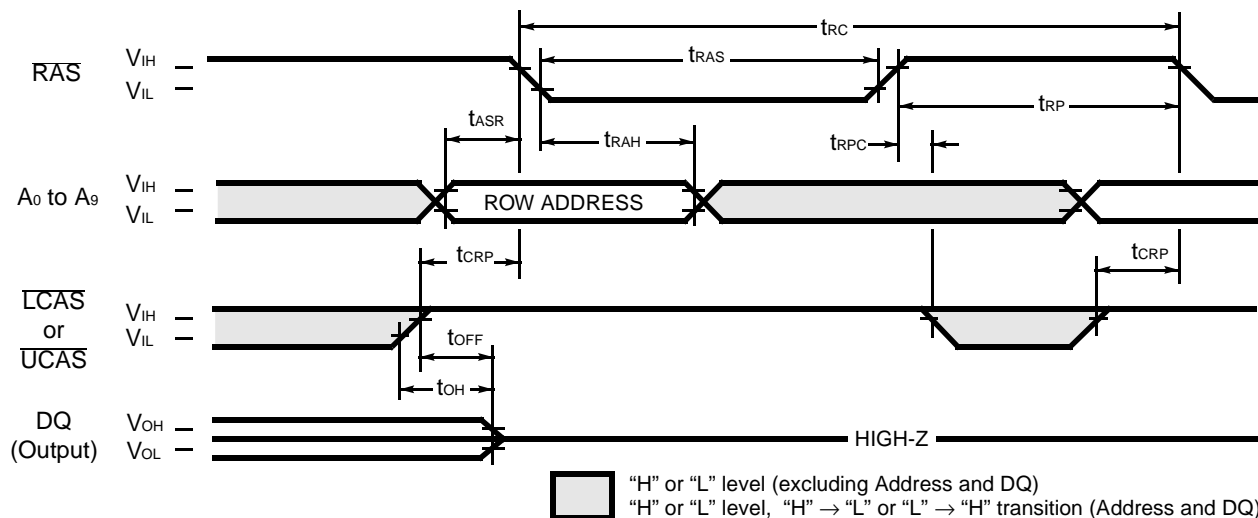
The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining RAS at a Low level and WE at a High level during all successive memory cycles in which the row address is latched. The address time is determined by tCAC, tAA, tCPA, or tOEA, whichever one is the latest in occurring.





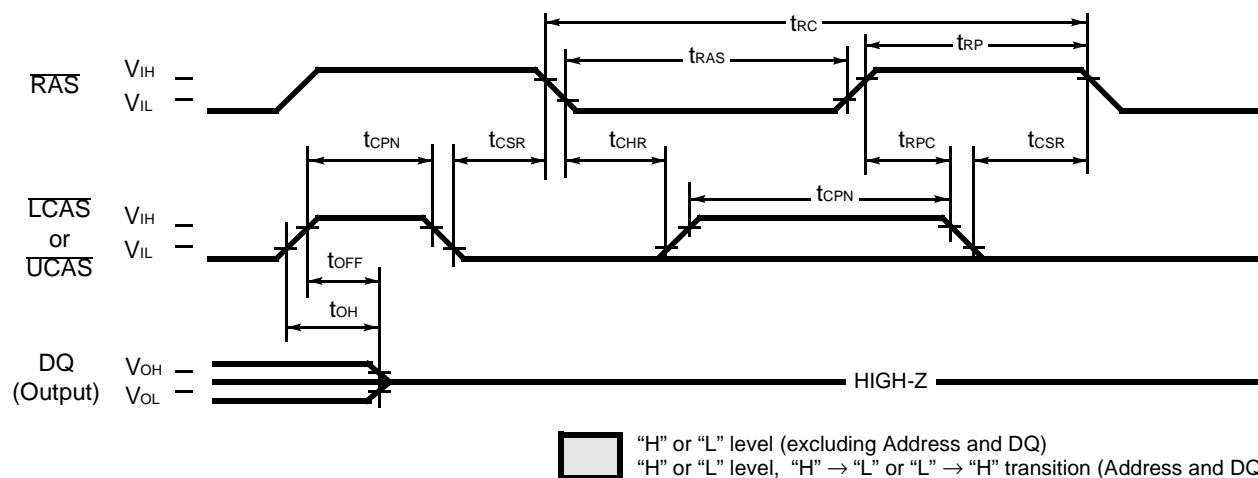


## MB81V18160B-50/-60/-50L/-60L

Fig. 13 -  $\overline{\text{RAS}}$ -ONLY REFRESH ( $\overline{\text{WE}} = \overline{\text{OE}} = \text{"H" or "L"}$ )**DESCRIPTION**

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1,024 row addresses every 16.4-milliseconds. Three refresh modes are available:  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh, and hidden refresh.

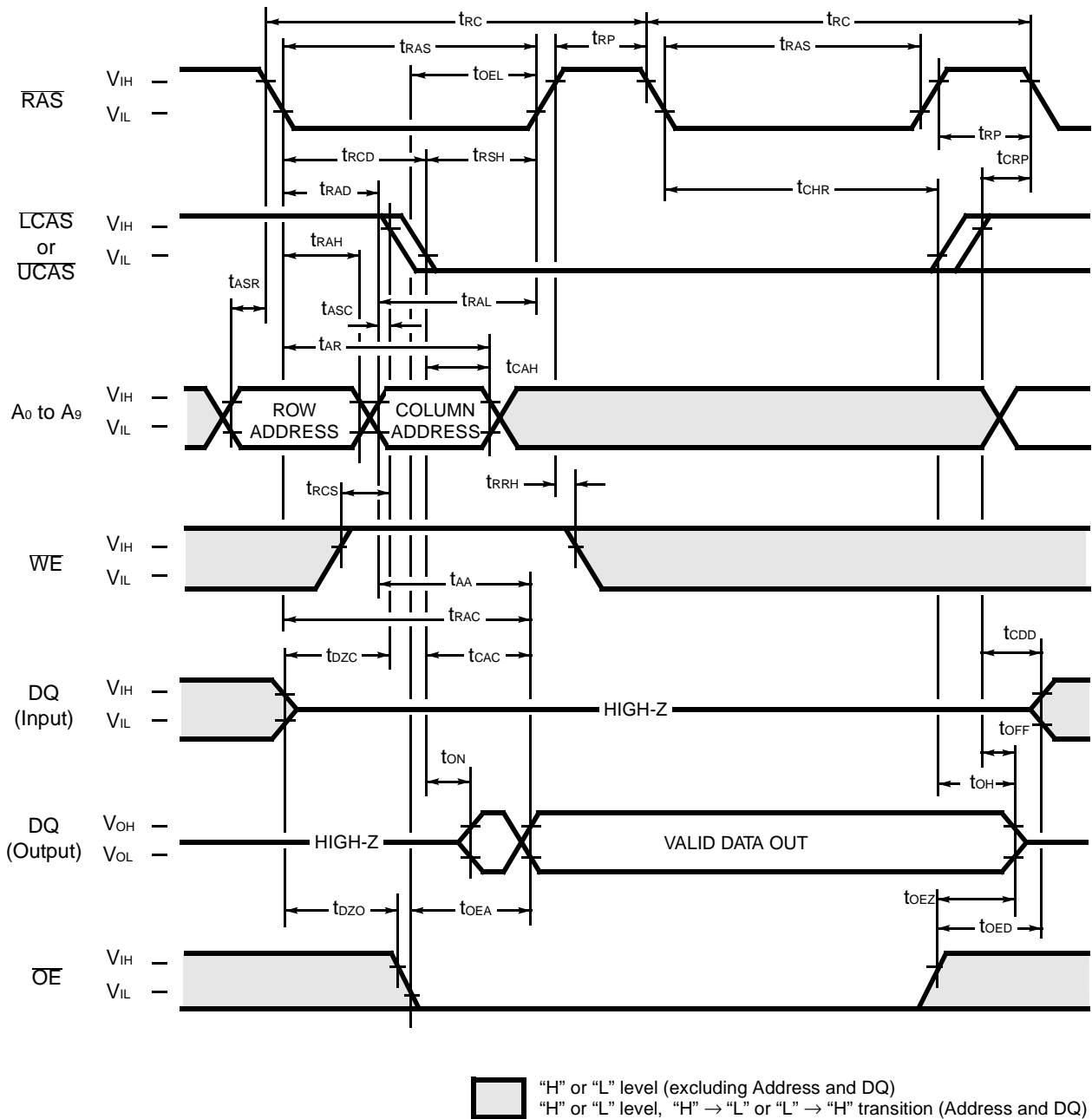
$\overline{\text{RAS}}$ -only refresh is performed by keeping  $\overline{\text{RAS}}$  Low and  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  High throughout the cycle; the row address to be refreshed is latched on the falling edge of  $\overline{\text{RAS}}$ . During  $\overline{\text{RAS}}$ -only refresh, DQ pins are kept in a high-impedance state.

Fig. 14 -  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH (ADDRESSES =  $\overline{\text{WE}} = \overline{\text{OE}} = \text{"H" or "L"}$ )**DESCRIPTION**

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  is held Low for the specified setup time ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh operation.

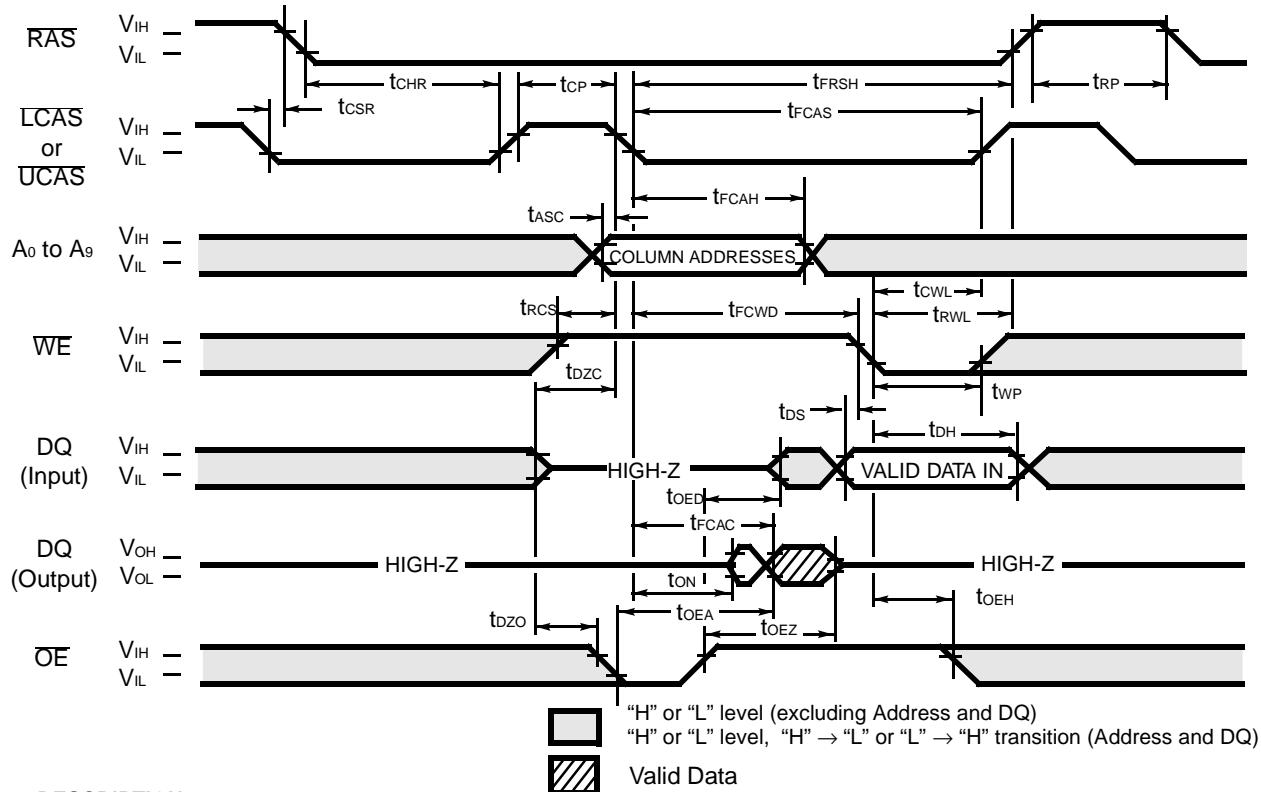
## MB81V18160B-50/-60/-50L/-60L

Fig. 15 – HIDDEN REFRESH CYCLE

**DESCRIPTION**

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  and cycling RAS. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have  $\overline{\text{CAS}}$ -before-RAS refresh capability.

## MB81V18160B-50/-60/-50L/-60L

Fig. 16 -  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH COUNTER TEST CYCLE**DESCRIPTION**

A special timing sequence using the  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test cycle provides a convenient method to verify the function of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh circuitry. If a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle  $\overline{\text{CAS}}$  makes a transition from High to Low while  $\overline{\text{RAS}}$  is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits  $A_0$  through  $A_9$  are defined by the on-chip refresh counter

Column Addresses: Bits  $A_0$  through  $A_9$  are defined by latching levels on  $A_0$  to  $A_9$  at the second falling edge of  $\overline{\text{CAS}}$ .

The  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Counter Test procedure is as follows;

- 1) Initialize the internal refresh address counter by using 8  $\overline{\text{RAS}}$ -only refresh cycles.
- 2) Use the same column address throughout the test.
- 3) Write "0" to all 1,024 row addresses at the same column address by using normal write cycles.
- 4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test (read-modify-write cycles). Repeat this procedure 1,024 times with addresses generated by the internal refresh address counter.
- 5) Read and check data written in procedure 4) by using normal read cycle for all 1,024 memory locations.
- 6) Reverse test data and repeat procedures 3), 4), and 5).

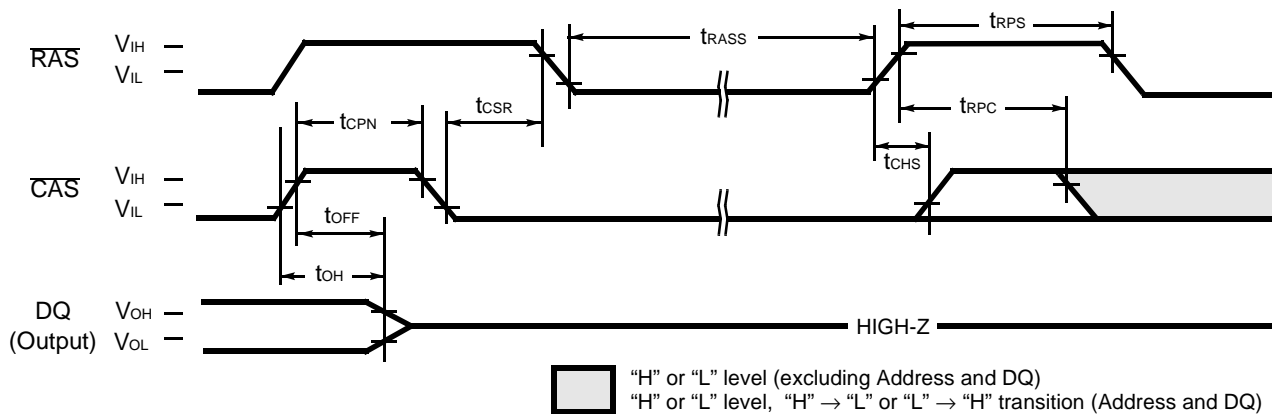
(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V18160B-50/50L		MB81V18160B-60/60L		Unit
			Min.	Max.	Min.	Max.	
60	Access Time from $\overline{\text{CAS}}$	$t_{\text{FCAC}}$	—	45	—	50	ns
61	Column Address Hold Time	$t_{\text{FCAH}}$	35	—	35	—	ns
62	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{FCWD}}$	63	—	70	—	ns
63	$\overline{\text{CAS}}$ Pulse Width	$t_{\text{FCAS}}$	45	—	50	—	ns
64	$\overline{\text{RAS}}$ Hold Time	$t_{\text{FRSH}}$	45	—	50	—	ns

**Note:** Assumes that  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test cycle only.

# MB81V18160B-50/-60/-50L/-60L

Fig. 17 – SELF REFRESH CYCLE ( $A_0$  to  $A_9 = \overline{WE} = \overline{OE} = \text{“H” or “L”}$ )



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V18160B-50L		MB81V18160B-60L		Unit
			Min.	Max.	Min.	Max.	
65	RAS Pulse Width	$t_{RASS}$	100	—	100	—	$\mu\text{s}$
66	RAS Precharge Time	$t_{RPS}$	90	—	110	—	ns
67	CAS Hold Time	$t_{CHS}$	-50	—	-50	—	ns

**Note:** Assumes Self Refresh cycle only.

## DESCRIPTION

The Self Refresh cycle provides a refresh operation without external clock and external Address. Self Refresh control circuit on chip is operated in the Self Refresh cycle and refresh operation can be automatically executed using internal refresh address counter and timing generator.

If  $\overline{CAS}$  goes to "L" before  $\overline{RAS}$  goes to "L" (CBR) and the condition of  $\overline{CAS}$  "L" and  $\overline{RAS}$  "L" is kept for term of  $t_{RASS}$  (more than 100  $\mu\text{s}$ ), the device can enter the self refresh cycle. Following that, refresh operation is automatically executed at fixed intervals using internal refresh address counter during  $\overline{RAS}=\text{“L”}$  and  $\overline{CAS}=\text{“L”}$ .

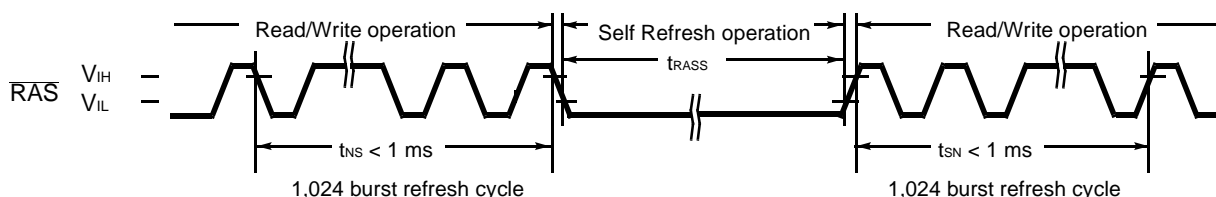
Exit from self refresh cycle is performed by toggling  $\overline{RAS}$  and  $\overline{CAS}$  to "H" with specified  $t_{CHS}$  min. In this time,  $\overline{RAS}$  must be kept "H" with specified  $t_{RPS}$  min.

Using self refresh mode, data can be retained without external  $\overline{CAS}$  signal during system is in standby.

Restriction for Self Refresh operation ;

For Self Refresh operation, the notice below must be considered.

- 1) In the case that distributed CBR refresh are operated between read/write cycles  
Self Refresh cycles can be executed without special rule if 1,024 cycles of distributed CBR refresh are executed within  $t_{REF\ max}$ .
- 2) In the case that burst CBR refresh or distributed/burst  $\overline{RAS}$ -only refresh are operated between read/write cycles  
1,024 times of burst CBR refresh or 1,024 times of burst  $\overline{RAS}$ -only refresh must be executed before and after Self Refresh cycles.



\* Read/Write operation can be performed non refresh time within  $t_{ns}$  or  $t_{sn}$ .

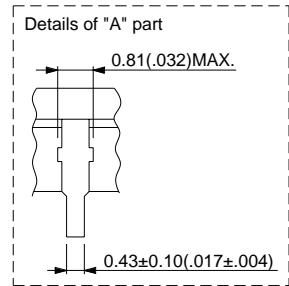
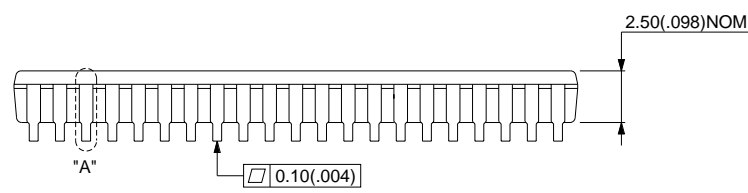
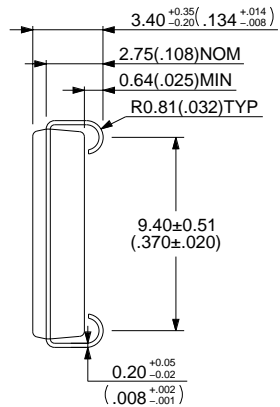
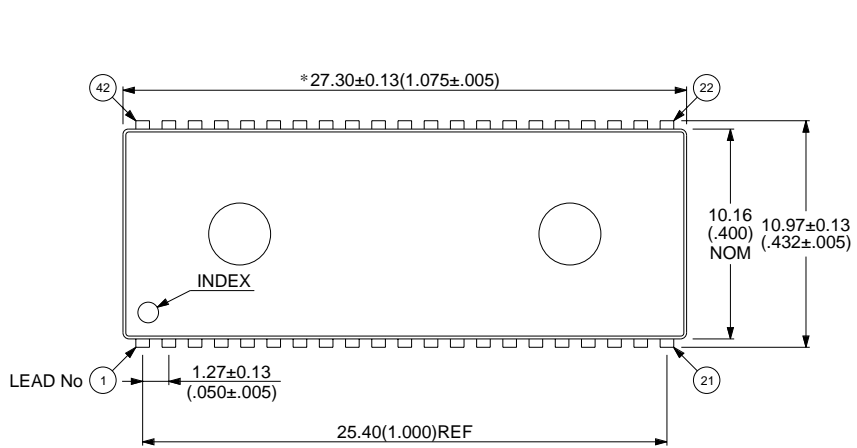


# MB81V18160B-50/-60/-50L/-60L

## ■ PACKAGE DIMENSIONS

42-pin plastic SOJ  
(LCC-42P-M01)

\*: Resin protrusion. (Each side: 0.15 (.006) MAX.)



© 1995 FUJITSU LIMITED C42001S-2C-1

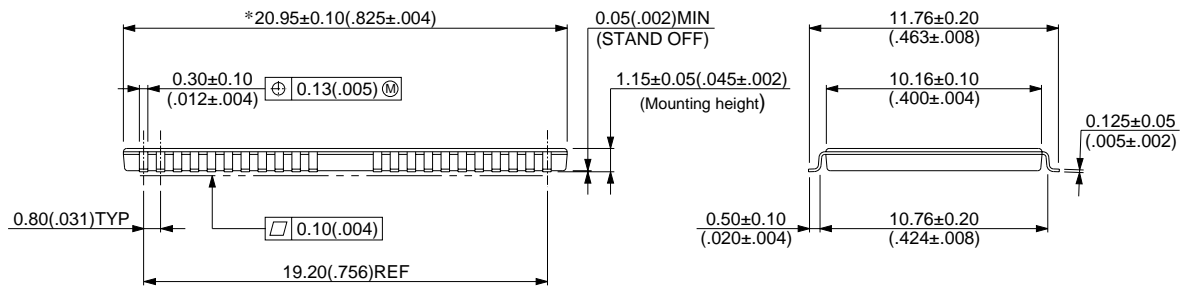
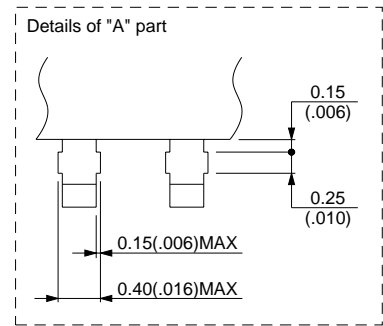
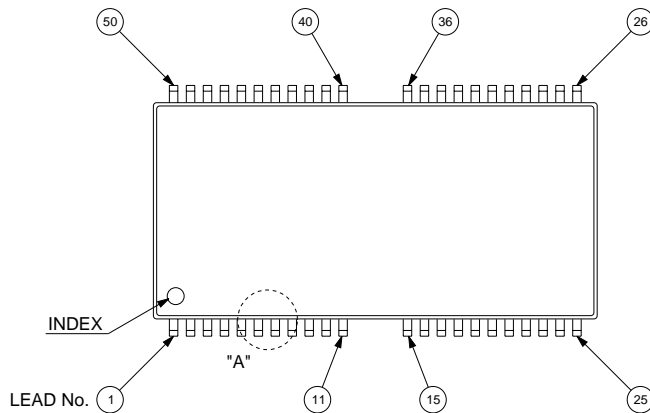
Dimensions in mm (inches)

# MB81V18160B-50/-60/-50L/-60L

(Continued)

50-pin plastic TSOP (II)  
(FPT-50P-M06)

\*: Resin protrusion. (Each side: 0.15 (.006) MAX.)



© 1994 FUJITSU LIMITED F50006S-2C-1

Dimensions in mm (inches)

# FUJITSU LIMITED

*For further information please contact:*

## **Japan**

FUJITSU LIMITED  
Corporate Global Business Support Division  
Electronic Devices  
KAWASAKI PLANT, 4-1-1, Kamikodanaka  
Nakahara-ku, Kawasaki-shi  
Kanagawa 211-88, Japan  
Tel: (044) 754-3763  
Fax: (044) 754-3329

<http://www.fujitsu.co.jp/>

## **North and South America**

FUJITSU MICROELECTRONICS, INC.  
Semiconductor Division  
3545 North First Street  
San Jose, CA 95134-1804, U.S.A.  
Tel: (408) 922-9000  
Fax: (408) 922-9179

Customer Response Center  
*Mon. - Fri.: 7 am - 5 pm (PST)*  
Tel: (800) 866-8608  
Fax: (408) 922-9179

<http://www.fujitsumicro.com/>

## **Europe**

FUJITSU MIKROELEKTRONIK GmbH  
Am Siebenstein 6-10  
D-63303 Dreieich-Buchsschlag  
Germany  
Tel: (06103) 690-0  
Fax: (06103) 690-122

<http://www.fujitsu-edc.com/>

## **Asia Pacific**

FUJITSU MICROELECTRONICS ASIA PTE LTD  
#05-08, 151 Lorong Chuan  
New Tech Park  
Singapore 556741  
Tel: (65) 281-0770  
Fax: (65) 281-0220

<http://www.fmap.com.sg/>

F9712

© FUJITSU LIMITED Printed in Japan

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

### **CAUTION:**

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.